C. McKinney
#6/Amdt A
8/25/00

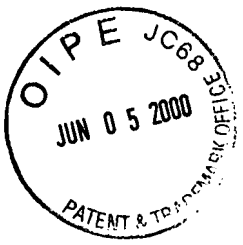
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

TOMITA et al.

Serial Number: 09/240,007

Filed: January 29, 1999



Group Art Unit: 2818

Examiner: Hoang, H.

For: SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

RESPONSE UNDER 37 C.F.R. 1.121

Commissioner for Patents
Washington, D.C. 20231

June 5, 2000

Sir:

In response to the Office Action dated February 3, 2000, the period for response having been extended until June 5, 2000, by the attached Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

A1

18. (Amended) A memory circuit receiving a clock signal and a strobe signal which have an identical cycle but have independent timings, comprising:

an address-input circuit which latches address signals in response to the [a] clock signal, and outputs the address signals in response to a timing signal;

a data-input circuit which latches data signals in response to the [a] strobe signal, and outputs the data signals in response to said [the] timing signal; and